ABSTRACT OF THE DISCLOSURE

In one embodiment of the invention, a system management interrupt (SMI) handler is invoked in response to an SMI. The SMI handler determines a thermal state of a processor. The SMI handler interacts with one of a speed step technology applet and a thermal driver in a thermal management operating system to transition the processor to one of a low power state and a high power state based on the thermal state according to a native performance control status.